REMARKS

Claims 5, 8, 10, 11, 33, 47, 48, 53, 54, 70, 71, 74, 75 and 82-87 are pending with claims 5, 8, 70 and 83 being independent. Claims 5, 8 and 70 have been amended, and claims 82-87 have been added. Support for the amendments and the new claims may be found, for example, at Fig. 1 of the application and the accompanying text. No new matter has been introduced.

Claims 5, 8, 33, 47, 48, 53, 54, 70-72, 74 and 75 have been rejected as being unpatentable over Okumura (U.S. Patent No. 5,945,972). Applicant requests reconsideration and withdrawal of this rejection for the reasons noted below.

First, applicant again requests reconsideration and withdrawal of this rejection because Okumura does not describe or suggest having a pixel include a source signal line and n TFTs (where n is a natural number equal to or greater than 2) connected to the source signal line, as recited in each of independent claims 5, 8 and 70. The rejection appears to respond to this argument by asserting that applicant had argued that Okumara does not describe connecting the gate electrode of SW1 to the source signal line 301, and by stating that such an arrangement is shown in Fig. 14 of Okumura.

Applicant agrees that Okumura shows having the gate electrode of SW1 connected to the source signal 301. However, applicant never asserted that this was not the case. Rather, applicant's position is that connecting the source signal to the gate of SW1, only one of which is included in a pixel, does not satisfy the recited connection of the source signal line to n TFTs, where n is a natural number equal to or greater than 2.

Second, applicant requests reconsideration and withdrawal of this rejection for the additional reason that Okumura does not describe or suggest having each of the n TFTs (where n is a natural number equal to or greater than 2) connected to the source signal line and a corresponding one of the n x m memory circuits (as recited in claims 5 and 70) or to the source signal line and an input terminal of a corresponding one of the n x m memory circuits (as recited in claim 8). Rather, Okumura, at Fig. 14, shows having SW1 connected to a signal line 301 and a memory circuit 321, and SW2 connected to the memory circuit 321 and a pixel cell.

Accordingly, for at least these reasons, the rejection should be withdrawn.

Claims 10 and 11 have been rejected as being unpatentable over Okumura in view of Nagao (U.S. Patent No. 6,380,876). Applicant again requests reconsideration and withdrawal of this rejection because Nagao does not remedy the failure of Okumura to describe or suggest the subject matter of claim 8 from which claims 10 and 11 depend.

Similarly to independent claims 5, 8 and 70, new independent claim 83 recites pixels that each include a first thin film transistor connected to a source signal line and a first memory circuit, and a second thin film transistor connected to the source signal line and a second memory circuit. Accordingly, claim 82 and its dependent claims are believed to be allowable at least because Okumura does not describe or suggest a pixel including multiple thin film transistors connected to a source signal line and memory circuits.

The fee in the amount of $790 in payment of the request for continued examination fee is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 4/24/06

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